I claim:

1. A semiconductor device having an improved contact to a conductive layer, comprising:

a. a first layer of conductive material;

b. a second layer of material having a contact hole therethrough on the first layer;

c. a localized thick region in the first layer subjacent the contact hole; and

d. a conductor contacting the thick region through the contact hole.

2. A semiconductor device according to Claim 1, wherein the thick region is positioned directly below the contact hole.

3. A semiconductor device having an improved contact to a conductive layer, comprising:

a. an underlayer of material having an opening therein;

b. a layer of conductive material formed on the underlayer and in the opening;

c. an overlayer of material on the layer of conductive material, the overlayer having a contact hole etched therethrough;

d. the opening being positioned, sized and shaped to form a localized thick region in the layer of conductive material subjacent the contact hole; and

e. a conductor contacting the thick region through the contact hole.

4. A semiconductor device according to Claim 3, wherein:

a. the conductive material has a Conformality C;

b. the layer of conductive material has a thickness T_1 at a location along a surface of the underlayer adjacent the opening;

c. the opening has a width W, where the width of the opening is determined from the equation: $W \leq 2 \times T_1 \times C$.

5. A semiconductor device according to Claim 4, wherein the conductive material is polysilicon having a conformality C of about 0.80.

6. A semiconductor device according to Claim 3, wherein the etch of the overlayer has a selectivity S with respect to the conductive layer and extends to a total effective depth D_{TE}, the contact hole has a nominal depth D_{CH}, the layer of conductive material has a thickness T_{CL} and the opening has a depth D, where D is determined from the equation: $D \geq (D_{TE} - D_{CH})/S - T_{CL}$.

7. A semiconductor device according to Claim 6, wherein the selectivity S is determined from the equation: $S = E_O/E_C$, where E_O is the rate at which the overlayer is etched and E_C is the rate at which the conductive layer is etched.

8. A semiconductor device according to Claim 3, wherein the etch of the overlayer has a selectivity S and extends to a total effective depth D_{TE}, the contact hole has a nominal depth D_{CH} and the thick region has a thickness T_{TR}, where T_{TR} is determined from the equation: $T_{TR} \geq (D_{TE}-D_{CH})/S$.

9. A semiconductor device according to Claim 8, wherein the selectivity S is determined from the following equation: $S = E_o/E_c$, where E_o is the rate at which the overlayer is etched and E_c is the rate at which the conductive layer is etched.

10. A semiconductor device according to Claim 3, further comprising a capacitor having a bottom electrode and a top electrode electrically isolated from the bottom electrode by a dielectric layer, wherein the layer of conductive material forms the top electrode and the conductor forms a contact through which a reference voltage is applied to the top electrode.

11. A semiconductor device, comprising:

a. a field effect transistor formed in a memory cell array region of a semiconductor substrate, the field effect transistor comprising a gate electrode formed on the substrate, and first and second source/drain regions formed in the surface of the substrate on opposite sides of the gate electrode;

b. a capacitor formed in the memory cell array region, the capacitor comprising a bottom electrode formed on the substrate in electrical contact with the first source/drain region, a dielectric layer formed on the bottom electrode, and a first region of a polysilicon top electrode formed on the dielectric layer over the bottom electrode;

c. a second region of the polysilicon top electrode formed in a peripheral region of the substrate adjacent to the memory cell array region;

d. an underlayer of material interposed between the substrate and the second region of the polysilicon top electrode in the peripheral region, the underlayer having an opening therein;

e. an insulating layer formed on the second region of the polysilicon top electrode, the insulating layer having a contact hole therethrough;

f. a conductor contacting the second region of the polysilicon top electrode through the contact hole; and

g. wherein the opening is positioned below the contact hole.

12. A semiconductor device according to Claim 11, further comprising a localized thick region in the second region of the polysilicon top electrode within the opening subjacent the contact hole.

13. A process for making a semiconductor device having an improved contact to a conductive layer, comprising the steps of:

a. forming a first layer of conductive material;

b. forming a second layer of material having a contact hole therethrough on the first layer;

c. forming a localized thick region in the first layer subjacent the contact hole; and

d. forming a conductor contacting the thick region through the contact hole.

14. A process for making a semiconductor device having an improved contact to a conductive layer, comprising the steps of:

a. forming an underlayer of material having an opening therein;

b. forming a layer of conductive material on the underlayer and in the opening;

c. forming an overlayer of material on the layer of conductive material and etching a contact hole therethrough;

d. forming a localized thick region in the layer of conductive material within the opening subjacent the contact hole; and

e. forming a conductor contacting the thick region through the contact hole.

15. A process for making a semiconductor device according to Claim 14, wherein:

a. the conductive material has a Conformality C;

b. the layer of conductive material has a thickness T_1 at a location along a surface of the underlayer adjacent the opening;

c. the opening has a width W; and

d. the width of the opening is determined from the equation: $W \leq 2 \times T_1 \times C$.

16. A process for making a semiconductor device according to Claim 14, wherein the etch of the overlayer has a selectivity S with respect to the conductive layer and extends to a total effective depth D_{TE}, the contact hole has a nominal depth D_{CH}, the layer of conductive material has a thickness T_{CL} and the opening has a depth D, where D is determined from the equation: $D \geq (D_{TE} - D_{CH})/S - T_{CL}$.

17. A process for making a semiconductor device according to Claim 16, wherein the selectivity S is determined from the following equation: $S = E_O/E_C$, where E_O is the rate at which the overlayer is etched and E_C is the rate at which the conductive layer is etched.

18. A process for making a semiconductor device according to Claim 14, wherein the etch of the overlayer has a selectivity S and extends to a total effective depth D_{TE}, the contact hole has a nominal depth D_{CH} and the thick region has a thickness T_{TR}, where T_{TR} is determined from the equation: $T_{TR} \geq (D_{TE}-D_{CH})/S$.

19. A process for making a semiconductor device according to Claim 18, wherein the selectivity S is determined from the following equation: $S = E_O/E_C$, where E_O is the rate at which the overlayer is etched and E_C is the rate at which the conductive layer is etched.

20. A process for making a semiconductor device according to Claim 14, further comprising the steps of forming a capacitor having a bottom electrode and a top electrode electrically isolated from the bottom electrode by a dielectric layer, wherein the layer of conductive material forms the top electrode and the conductor forms a contact through which a reference voltage is applied to the top electrode.